A 1.5-V 4-GHz Dynamic-Loading Regenerative Frequency Doubler in a 0.35-μm CMOS Process

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Abstract — **This paper proposes a new topology of a frequency doubler using a dynamic-loading technique to achieve higher operating frequency, larger output swing, larger bandwidth and lower phase noise compared to traditional designs. Implemented in a standard 0.35-μm digital CMOS process and at a 1.5-V supply, the proposed frequency doubler measures a maximum operating output frequency of 4 GHz with a bandwidth of 2.4 GHz while consuming a power of 3.7mW. The single-ended output amplitude is ranging from –3.0 to -6.5 dBm, and the phase noise is as low as –111dBc/Hz @ 500kHz offset.**

I. INTRODUCTION

Frequency synthesizer is one of the important building blocks to generate a reference frequency for wireless communication systems. Because of the increasing demand for connectivity with higher and higher speed, frequency synthesizers with higher operating frequency are desired. One attractive solution is to use frequency doublers at the output of the synthesizers to achieve the desired output frequency while effectively reducing the VCO output frequency by half.

Two existing approaches are being used to implement the frequency doubling circuit. The first approach is the use of an analog multiplier or up-conversion mixer with the two input terminals connected together [1]. The main problem is that the output swing is typically limited to only around several tens of mill-volt which is not large enough to drive the next stage. In addition, such a design requires passive component such as inductor or resistor and thus occupies a large chip area.

The second approach is to use regenerative frequency doubling technique using essentially a two-stage ring oscillator [2]. Each of the differential amplifiers is a simple emitter coupled differential pair with resistive loads. Although such a frequency doubler can operate at a high frequency, the resistive loading inevitably limits the operating bandwidth, which is defined as the difference between the maximum and the minimum operating frequencies. Moreover, to achieve the desired frequency, such a frequency doubler has so far only been implemented in advanced BJT processes.

This paper presents a new dynamic-loading technique to implement a CMOS frequency doubler with a high operating frequency, a large bandwidth, a high output swing and a low phase noise. Implemented in a standard digital 0.35-μm CMOS process, a 4-GHz frequency doubler with a 1.2-GHz bandwidth is designed and demonstrated at a 1.5-V supply voltage.

II. Circuit Description

The block diagram of the proposed dynamic-loading regenerative frequency doubler is shown in Figure 1. It is essentially a two-stage cross-coupled ring oscillator. The corresponding detailed schematic diagram is shown in Figure 2. Each of the amplifier stages is a simple differential pair with PMOS dynamic loading (Mp_1, Mp_2). The dynamic-loading technique enables a larger bandwidth compared to the resistive loading. Since the RC time constant at the output nodes of the differential amplifiers is changing dynamically, it offers a large bandwidth at that output node. Furthermore, the absolute value of the resistive load cannot be controlled very well in CMOS technology, which would affect the operating frequency of the doubler. This problem does not exist or at least is minimized when PMOS dynamic loading is being used.

In the conventional dynamic-loading technique, the input clocks of the gate (Mp_1, Mn_4) are complementary. However, the phase difference is $\pi/2$ for the proposed frequency doubler. The idea is known as negative skewing [3]. The simplified conceptual diagram is shown in Figure 3. The clock input of the Mp_1 turns on before low-to-high output transitions and turns off the PMOS before

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high-to-low output transitions. It speeds up the transitions and offers a larger swing at the output nodes of the differential amplifiers, which in turn larger output swing of the frequency doubler.

In our proposed doubler shown in Figure 2, the cross-coupled pair (Mn_1, Mn_2) provides a positive feedback to maintain oscillating at the output nodes of the differential amplifiers. Both differential amplifiers are sharing the same current biasing transistor (Mn_3). This technique can help to improve the amplitude and phase matching at the output nodes of the amplifiers [4]. A differential pair (Mn_4, Mn_5) is used to maintain quadrature phase of the output nodes of the amplifiers. More importantly, it is the component to double the input frequency.

The nonlinear characteristic of the differential pairs (Mn_4, Mn_5) produces a large double-frequency output signal at the drains of Mn_6 and Mn_{11}. Since a large swing occur at the output nodes of the differential amplifiers and the current biasing transistor is biased at the pinch-off region, the double-frequency signal is maximized. Moreover, the outputs of frequency doubler are exactly out of phase since the (Mn_4, Mn_5) and (Mn_9, Mn_{10}) are cross-coupled to each other. Effectively, the idea of the frequency doubling can be thought of as two signals being mixed together by Mn_4 as shown in Eq.1.

$$a\sin\omega t \cdot a\sin(\omega t + 90^o) = \frac{a^2 \sin 2\omega t}{2} \quad (1)$$

where a is the amplitude of the amplifier's output strength.

From Eq. 1, the double-frequency output signal amplitude is equal to $a^2/2$. Consequently, in order to maximize the output swing of the doubler, the output swing of the differential amplifiers needs to be maximized.

In practical situation, the phase difference is not exactly 90°. Lets assume a small phase difference error $\Delta\theta$. Since the error $\Delta\theta$ is really small, the first term in Eq. 2 approximately equals to that predicted in Eq. 1. At the same time, the second term in Eq. 2 becomes negligibly small.

$$\begin{aligned} & a\sin\omega t \cdot a\sin(\omega t + 90^o + \Delta\theta) \\ &= \frac{a^2 \sin 2\omega t \cos\Delta\theta}{2} - a^2 \sin^2 \omega t \sin\Delta\theta \end{aligned} \quad (2)$$

The core circuit of the doubler is extremely small because no passive component is used. Thus, it is more suitable for monolithic integration. Finally, the output signal has low spurs at the fundamental frequency and there is no need for any filtering to extract out the double-frequency signal.

III. Measurement Results

The proposed frequency doubler is fabricated in a standard 0.35-μm CMOS process. The threshold voltages of the PMOS and NMOS transistors are 0.77V and 0.6V respectively. A die photo is shown in Figure 4, and the core chip area is only 79μm x 74μm.

The doubler is measured at 1.5-V supply with a power consumption of 3.7 mW. The maximum output operating frequency is measured to be 4 GHz with a 2.4-GHz output bandwidth. Figure 5 shows a plot of the single-ended output signal power at different output frequencies. The output power is ranging from –3.0 dBm to –6.5 dBm which is relatively constant. The buffered output spectrum at 4-GHz output frequency and its close-in spectrum are shown in Figure 6. The fundamental frequency signal at the output of the doubler is much larger than that predicted by Eq. 2 mainly because of the direct coupling from the input to the output. The measured coupling of the fundamental frequency is around –60dBc. Including all the loss from the on-chip output buffer and the testing setup (the loss at 2GHz and 4GHz are measured to be around –24dB and –30dB respectively), the effective coupling is approximately –30dBc.

Figure 7 shows a logarithmic plot of the measured output phase noise at different offset frequencies with a 4-GHz center frequency. Figure 8 shows the output signal phase noise and the input signal phase noise at different input frequencies. The output phase noise degrades around 6dB when compared to the input phase noise. At the maximum output frequency (4 GHz), the output phase noise is measured to be –102dBc/Hz at 100kHz offset and –106dBc/Hz at 500kHz offset. Since the phase noise is measured at single-ended outputs, an improvement of 3dB is expected if the phase noise is measured differentially.

The doubler is also measured at 1.2-V supply with a power consumption of 2 mW. Figure 9 shows the singled-ended output signal power at different output frequencies. The output power is ranging from –4.2dBm to –7.5dBm which is smaller than in case of 1.5-V supply mainly due to smaller output swing of the differential amplifiers. The maximum output operating frequency is around 2.8 GHz with 1.2GHz output bandwidth. Figure 10 is the output signal phase noise and input signal phase noise at different input frequencies.

IV. Conclusion

Table 1 summarizes the measured performance of the proposed divider together with that of the recently reported divider designs for comparison. The proposed doubler is capable to operate at a frequency of 4GHz with a bandwidth of 2.4 GHz at a 1.5-V supply voltage using a standard 0.35-μm CMOS process.

References

[1] Y. K. Seng, S. S. Rofail, "Design and analysis of a ±1V CMOS four-quadrant analogue multiplier," IEE Proc-Circuits Devices Syn, vol. 145, No. 3, June 1998

[2] J. Maligcorgos and J. R. Long, "A 2-V 5.1-5.8-GHz image-reject receiver with wide dynamic range", ISSCC, 2000, pp.322-323.

[3] S. Lee, B. Kim and K. Lee, "A novel high-speed ring oscillators for multiphase clock generation using negative skewed delay scheme," JSSCC, 1997, pp.289-291

[4] C. W. Lo and H. C. Luong, "2-V 900-MHz Quadrature Coupled LC Oscillator with Improved Amplitude and Phase Matchings," ISCAS, June 1999.

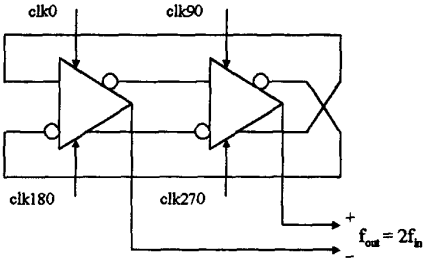


Figure 1 Block diagram of the proposed frequency doubler

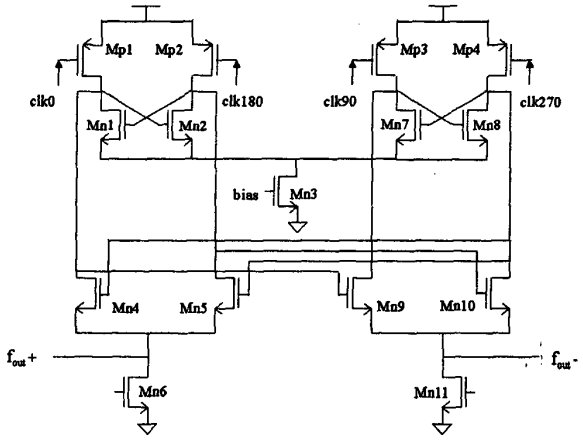


Figure 2 Schematic diagram of the proposed frequency doubler

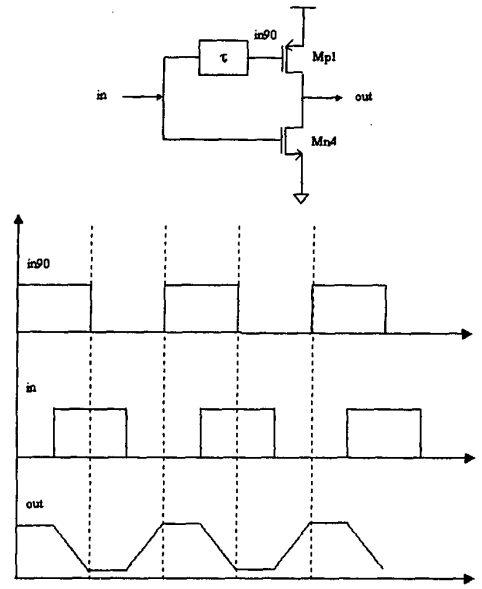


Figure 3 The idea of negative skew

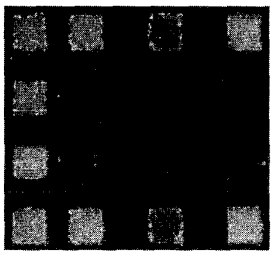


Figure 4 Die photo

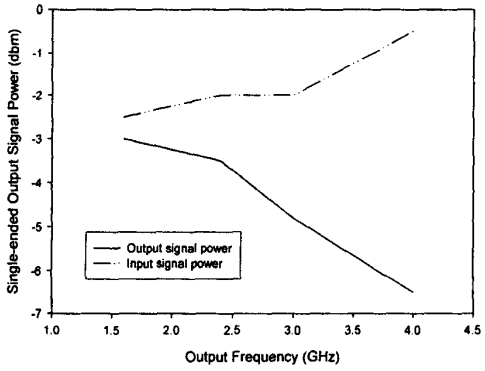
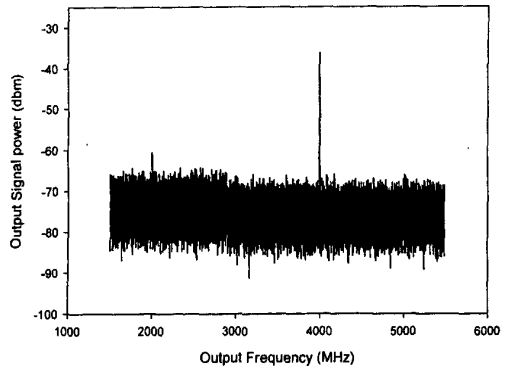


Figure 5 Output signal power at different output frequencies with 1.5V supply



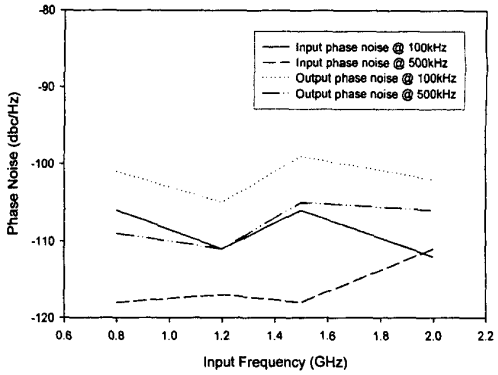


Figure 8 Phase noise of different input frequencies with 1.5V supply

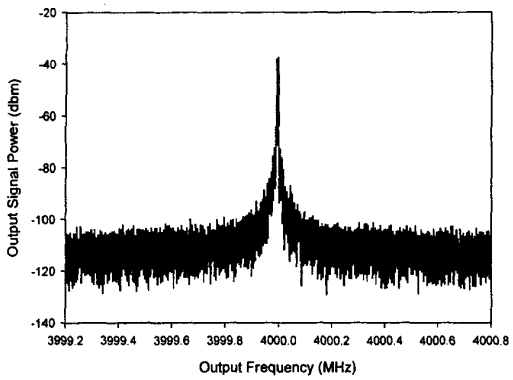


Figure 6 Measured output power spectrum at 4GHz output frequency with 1.5V supply
(a) whole spectrum (b) close-in spectrum

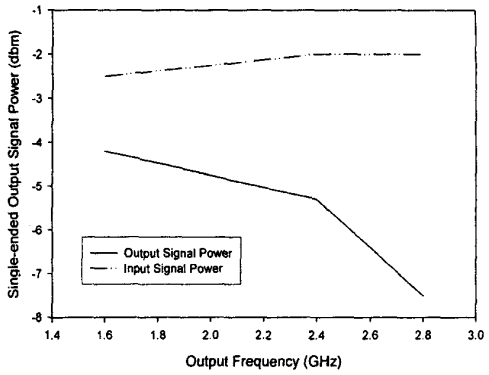


Figure 9 Output signal power at different output frequencies with 1.2V supply

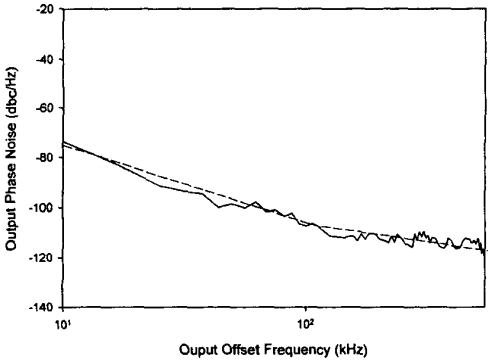


Figure 7 Measured output phase noise for 4GHz output frequency with 1.5V supply

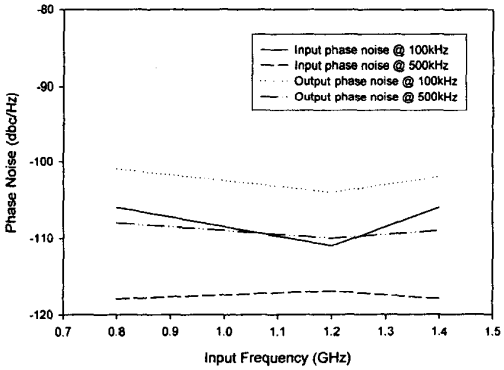


Figure 10 Phase noise at different input frequencies with 1.2V supply

Table 1. Comparison of recently published frequency doubler

	Y. K. Seng [1]	J. Maligcorgos [2]	Proposed doubler
Technology	0.8μm CMOS	0.5μm BJT	0.35μm CMOS
Voltage Supply	± 1V	2.2V	1.5V
Maximum Output Operating Frequency	37kHz	6GHz	4GHz
Output Bandwidth	/	1GHz	2.4GHz
Input Signal Strength	-20dbm	/	-1 to -3dbm
Output Signal Strength	-22dbm	/	-3 to – 6.5dbm
Power Consumption	37μW	/	3.7mW